APPLICATION NOTE

Application information for the TDA6118JF S1 wide band video output amplifier

AN01031

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Abstract

This report gives a description of the TDA6118JF S1 wideband video output amplifier together with application aspects.

Application of the TDA6118JF S1 wideband video output amplifier AN01031 Version: 2.0

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Summary

This note gives the application description of the TDA6118JF S1 wideband video output amplifier and provides the user with basic hints to obtain an optimal performance in the application.

The following application aspects will be described:
- External components calculation.
- Circuit application & Application hints.
- Flashover protection.

In the appendix the following items are described:
- An interface socket is described to quickly refit a TV set equipped with the TDA6120Q with the TDA6118JF S1 concept for evaluation purposes.
- A video concept for typical TV applications, using the combination TDA933X (monolithic display processor) and the TDA6118JF.

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1. INTRODUCTION

The aim of this application note is to describe the basic operation of the TDA6118JF S1, further called TDA6118JF in this application note. The TDA6118JF is a wide band video output amplifier and to provide the user with basic hints to gain an optimal performance in the application. The TDA6118JF includes one video output amplifier in a plastic DIL-bent -SIL medium power package DBS9MPF, using high-voltage DMOS technology, and is intended to drive a CRT in a high demanding market of High Resolution TVs. The TDA6118JF is provided with a black current stabilisation data pin.
The TDA6118JF needs an external flash diode.

The TDA6118JF is pin aligned (not compatible) with the TDA6111Q.

For set makers using the TDA6120Q, a TDA6118JF interface socket can be applied to quickly refit a “TDA6120Q set" to a TDA6118JF evaluation set. This information is given in the appendix of this report.

The main features of the TDA6118JF are:

- High large signal bandwidth: 17 MHz at $100V_{PP}$.
- Rise / fall times: 21ns at $100V_{PP.}$
- Bandwidth independent of voltage gain.
- Selectable gain of 50/80.
- Selectable output black level 126/155V.
- Current measurement output for automatic black current stabilisation (ABS).
- High power supply rejection ratio.
- Protection against ESD.
- Low static power dissipation.
- Thermal protection.
- Very simple application, due to high level of integration.

1.1 Block diagram description.

The complete block diagram of the TDA6118JF is shown in Figure 1.

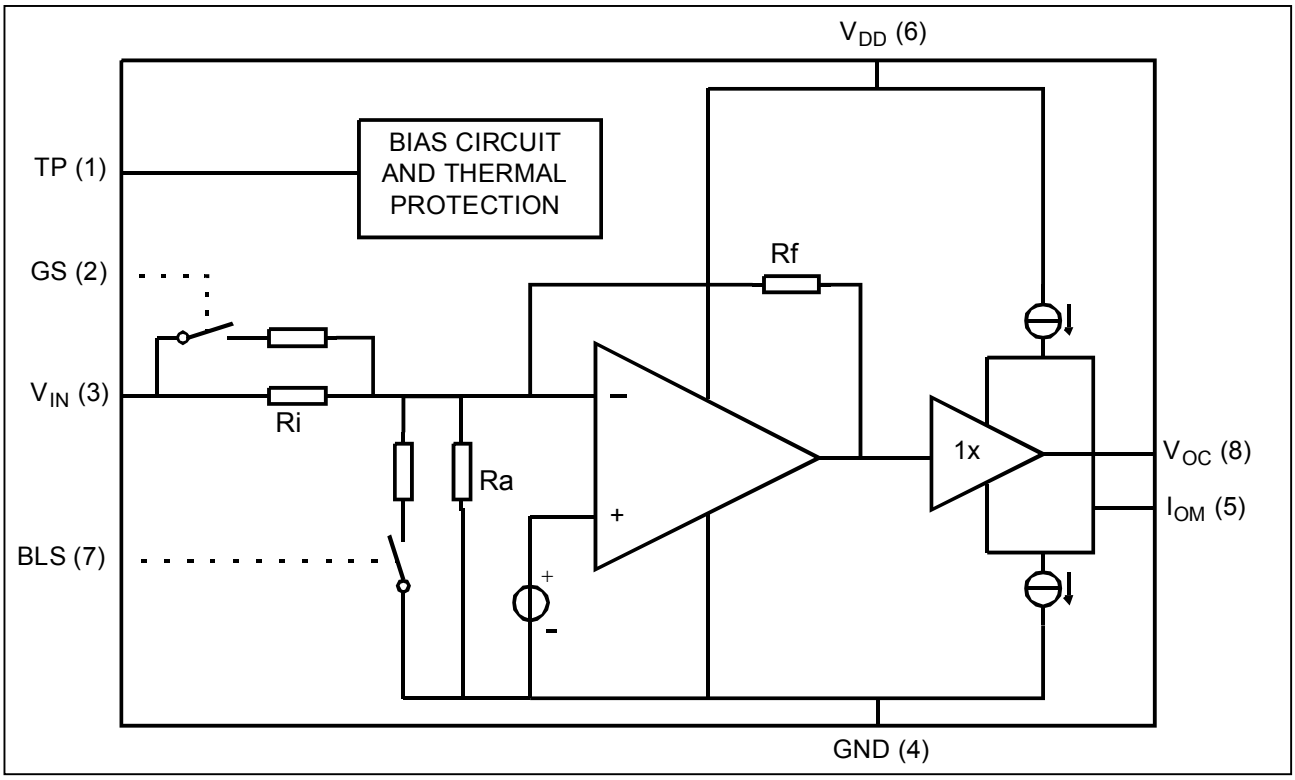

Figure 1: Block diagram of the TDA6118JF.

The TDA6118JF consists of one monolithic video output amplifier and can be seen as an operational amplifier with negative feedback. Furthermore the TDA6118JF has an internal thermal protection circuit that decreases the bandwidth at high temperatures and the TDA6118JF needs only one power supply voltage (V_{DD}).
In contrast to previous video amplifier IC's, the external resistors (Rf, Ri and Ra) are integrated which saves 3 resistors per channel, so 9 resistors per system. The TDA6118JF offers the possibility to change the values of Ri and Ra by means of the gain and a black level select pin (pin 2 GS and pin 7 BLS). The reference voltage is integrated, which saves an extra resistor divider and a decoupling capacitor, so the integration level of the TDA6118JF is very high. In comparison with previous video amplifiers, another advantage of the TDA7118JF is the less sensitivity for parasitic capacitances on the PCB, due to the high level of integration.

An external protection diode must be applied between de pin 8 V_{OC} and pin 6 V_{DD}. This diode prevents that high voltage spikes damage the amplifier during a picture tube flashover.

The TDA6118JF is equipped with a black current stabilisation output (pin 5 I_{OM}). When using RGB-processor with a black current input as driver no adjustments are required for gain and black setting.

The pinning of the TDA6118JF is pin aligned (don't read pin compatible) with the TDA6111Q.

The simplified basic application diagram of theTDA6118JF is given below in Figure 2.
The complete application diagram of theTDA6118JF is given in Figure 8.

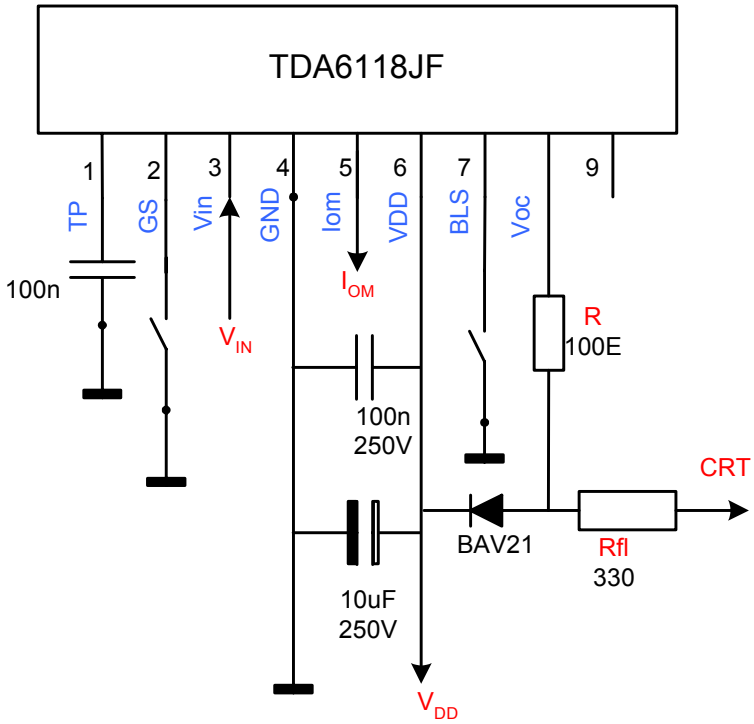

Figure 2: Simplified basic application of the TDA6118JF.

1.2 Functional pin description.

A functional pin description is given in this chapter.

Pin 1. Thermal protection (TP).
This pin is used for synchronization of the three channels and should therefore be connected to the TP pins of the other channels. This synchronization prevents colour shifting if the thermal protection of one amplifier is active. There will be a dc level present at this pin, which represents the temperature of the device. To keep this pin free of interference, it must be decoupled to ground by means of a capacitor (100nF/50V).

Pin 2. Gain select (GS).
If this pin is open the gain is 80 and when connected to GND the gain will be 50. The pin is internally connected to a supply rail by means of a pull-up resistor, therefore it is allowed to keep this pin floating.

Pin 3. Inverting input (V_{IN}).
The input configuration consist of a resistor Ri connected to the negative input of an operational amplifier and has a DC level of 2.5 V which is directly related to the internal reference voltage of 2.5V.

Pin 4. Ground (GND).
The grounding of the application is extremely important for good flash robustness, see section 5.1

Pin 5. Black current measurement output (I_{OM}).
This pin is the automatic black current stabilisation (ABS / AKB) output. The voltage on this pin is limited by an internal zener diode of approximately 7V. If black current measurement is not needed, pin 5 I_{OM} can be connected to small signal ground.

Pin 6. High-voltage supply (V_{DD}).
This is the voltage supply pin of the device and has to be decoupled to ground by means of a capacitor for good flash robustness, see section 5.1.

Pin 7. Black level select (BLS).
By means of this pin it is possible to adapt the black level output voltage to the required level for the CRT. If this pin is open the output voltage is 155V at 2.5V input. When connected to GND, the output voltage is 126V at an input voltage of 2.5V. The pin is also internally connected by a pull-up resistor to a supply rail, and therefore this pin can be floating.

Pin 8. Cathode output (V_{OC}).
The output current is delivered by a quasi complementary class-A/B push-pull stage designed in DMOS technology and can source and sink a current of 70mA for video output voltages of $100V_{PP}$ with rise and fall times of 21 ns. The output stage has a minimum saturation voltage of max. 17V@7mA. The maximum voltage of the output stage is min. V_{DD} -18V. This output pin has to be connected to the cathode of the CRT via a flashover protection resistor, which limits the current towards the amplifier. A high surge clamping diode has to be applied externally from this output to pin 6 V_{DD}.

Pin 9. Not connected.

1.3 Internal pin configuration

The internal pin configuration of the TDA6118JF is given in Figure 3.

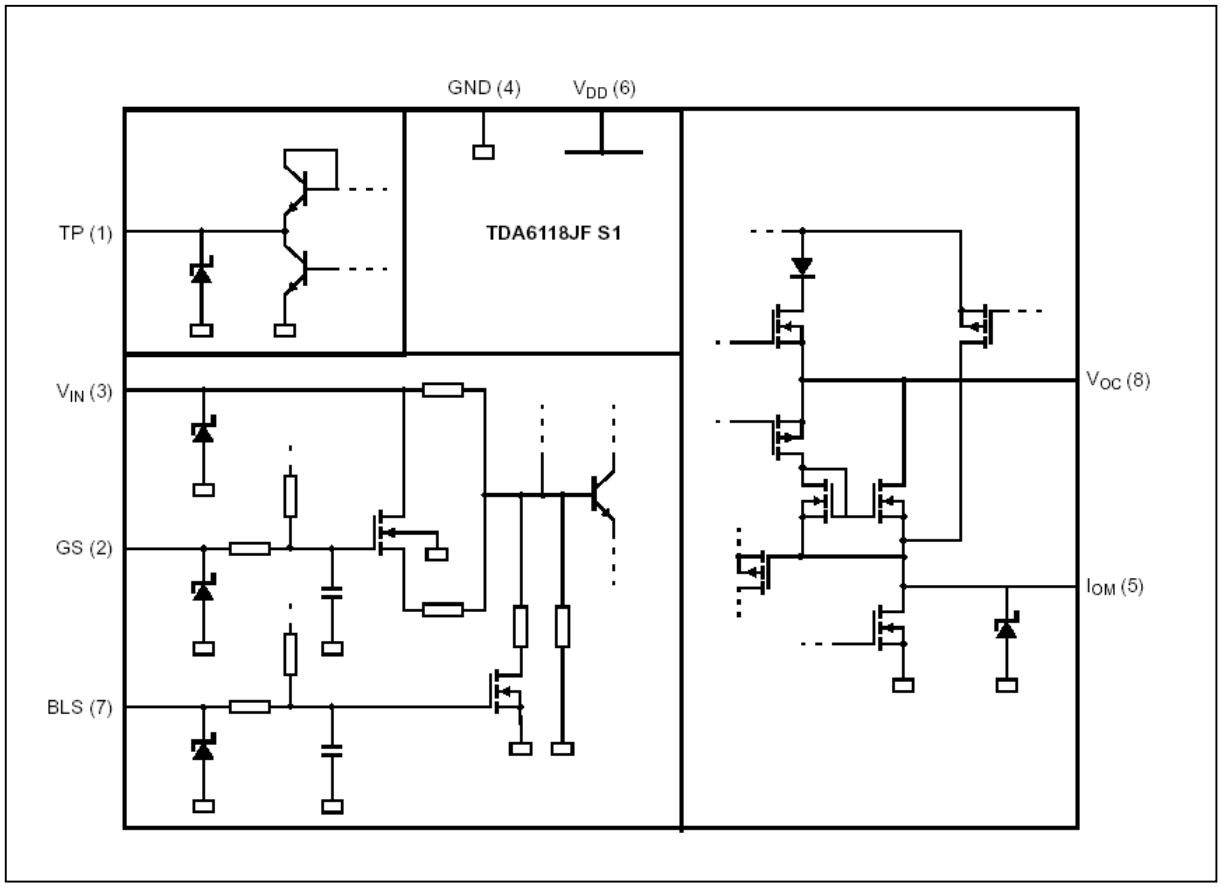

Figure 3: Internal pin configurations of the TDA6118JF

2. DESIGN CONSIDERATIONS.

2.1 Amplifier part.

The applied video output amplifier in the TDA6118JF is a negative current feedback amplifier. The basic characteristics of this operational amplifier will be explained shortly.

The general negative - feedback topology is depicted in Figure 4.

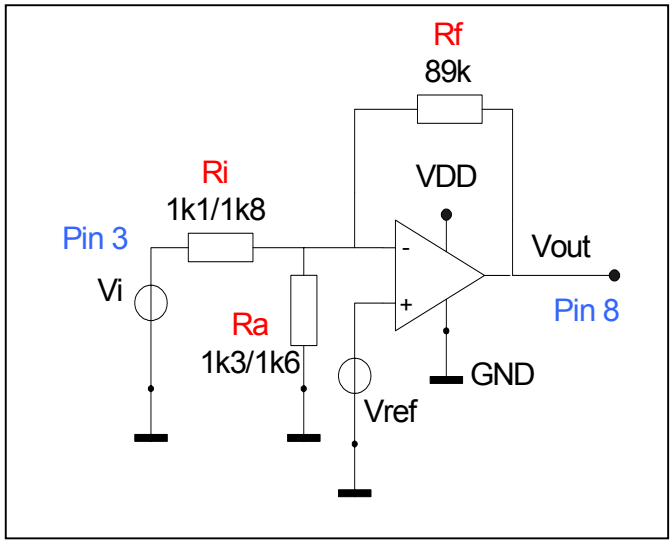

Figure 4: Basic configuration of the video amplifier.

It incorporates an operational amplifier with a differential input (V^+ and V^-) and a single ended voltage output. The input of the overall amplifier is V_I. V^+ is connected to an internal reference voltage (V_{REF}). The reference voltage (V_{REF}) is very stable regarding temperature drift. In contrast to previous types of DMOS amplifiers, the resistors R_I, R_A and R_F are all integrated in the TDA6118JF.

2.2 Voltage gain

The voltage gain is defined by:

Equation 1

$$Av = -\frac{Rf}{Ri}$$

This voltage gain is independent of R_A, the derivation for this equation can be found in Appendix A. The value of the internal feedback resistor R_F is fixed, and the gain can be lowered by means of grounding the gain select (GS) pin. If this pin is connected to ground, it changes the value of R_I so that the gain lowers. The value of R_F is fixed to 89kΩ. The input resistance can be switched between 1.1kΩ and 1.8kΩ, consequently the gain is 80* or 50*. For most RGB-processors e.g. TDA933X a voltage gain of 50 is sufficient to get $100V_{PP}$ video output signals.
When for EMC reasons an external resistor is placed in series with the input, this will affect the gain as well. The value of R_I will be increased with the value of the external resistor and therefore the gain will be lowered.

The new voltage gain can be calculated with Equation 2.

Equation 2

$$Avnew = \frac{Av * RISPEC}{RISPEC + RS}$$

Where:

AV_{NEW} is the new voltage gain.
AV_{SPEC} is the gain selected with the GS pin, so 50 or 80.
R_{ISPEC} is the input resistance chosen with the GS pin, so 1.8kΩ or 1.1kΩ.
R_S is the added series resistance.

We do not recommend to add these extra series resistance, because there will be a bigger spread in gain between products due to the spread in R_I.

2.3 DC to DC transfer related to cut-off level

If the input voltage of the amplifier equals the reference voltage, the output voltage is defined by:

Equation 3

$$Vout = Vref\left(\frac{Rf}{Ra} + 1\right)$$

The derivation of this equation is given in Appendix B.

The value of R_F is fixed due to the chosen gain. V_{REF} is determined by a very stable bandgap voltage source, so only the value of R_A is responsible for the black level voltage.

The value of R_A is chosen so, that the nominal black level output of de RGB-processor will result in a voltage near the cut off voltage of the CRT.

When connecting the black level select pin to ground, R_A will have a value of 1.7kΩ, which results in a black level of 126V. Leaving this pin floating, R_A will have a value of 1.4 kΩ resulting in a black level of 155V.

The output voltage at a given input voltage can be found in the datasheet of the TDA6118JF on page 6.
More accurate is to calculate it by means of Equation 4

Equation 4

$$Vout = (Vref - Vin) \cdot Av + Vocnom$$

Where:

V_{OUT} is the output voltage.
V_{REF} is the internal reference voltage, so 2.4V.
V_{IN} is the input voltage.
A_V is the selected voltage gain, so 50* or 80*.
V_{OCNOM} is the selected nominal black level output voltage, so 126V or 155V.

2.4 Thermal protection

The TDA6118JF is provided with an internal temperature protection, therefore preventing thermal ageing and guaranteeing optimal performance during the television's lifetime.
Another benefit is that the heatsink can be designed for practical values instead of worst-case conditions.

The protection decreases internal quiescent current if the die temperature becomes too high. As a result the bandwidth will be limited and thus limiting the dynamic dissipation.

At a die temperature of 145°C the bandwidth will be typically decreased by 25%

To prevent drifting of the colour temperature (colour shift) the thermal protection of the three guns must be synchronised with each other. This is done by connecting the TP pin's of the channels together. Furthermore there should be a 100nF decoupling capacitor present from this connection to the small signal ground.

2.5 Black current stabilisation (AKB) / continuous cathode calibration

Pin 5 I_{OM} of the TDA6118JF, the black current stabilisation data pin, is a current source which delivers a copy of the real cathode current of the CRT when 1.8V<Vom<6V. This current can be driven directly into the black current input pin of an RGB-processor. Depending on the RGB-processor, sometimes a small interface has to be applied.

The simplest application of the TDA6118JF in an automatic black current stabilisation set-up in conjunction with an RGB processor is shown in Figure 5. The black current stabilisation loop is an automatic control loop which stabilises the black current of each channel sequentially and independently every field. When using an RGB-processor e.g. TDA933X, the loop is active for a four-line period, immediately after the end of the field blanking. During field scan (outside the 4L black current measuring time), the normal video current flows in the ABS feedback path. To prevent high video currents from flowing in the processor black current input, the voltage on pin 7 of the TDA6118JF is limited by an internal zener diode of 7V. The black current input of the TDA933X has a low impedance current driven input with leakage current compensation.

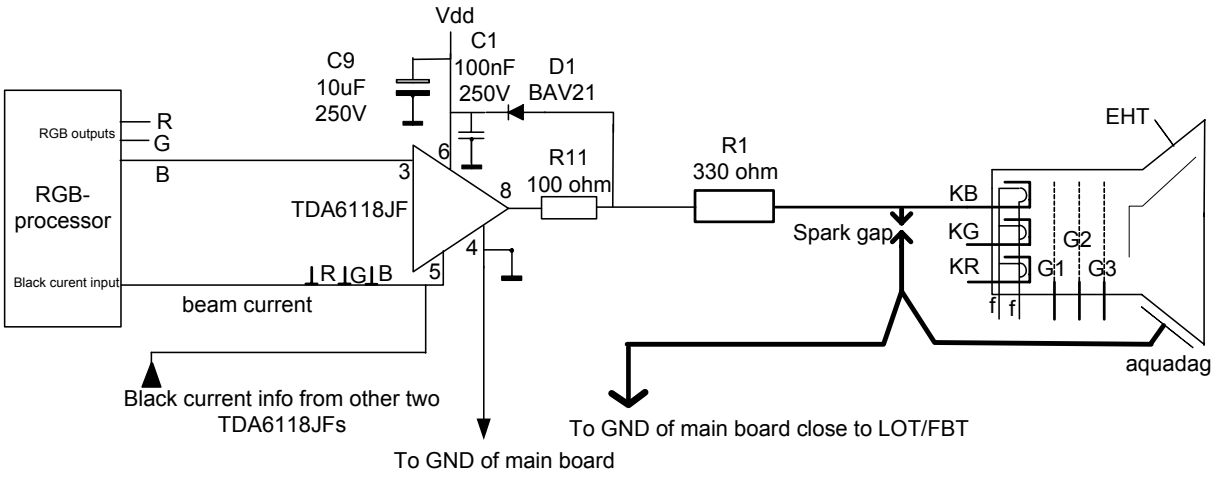

Figure 5: Black current stabilization application with an RGB processor and the TDA6118JF

It is also possible to use this pin for discharging the CRT after a switch off. Most video-processors are equipped with the possibility to connect a fixed current source to the I_{OM} input, so that the CRT will be discharged for a given time with a constant current. This prevents stray emission. The I_{OM} pin of the TDA6118JF can be used in this configuration. The discharge current can be up to 5mA

3. Dissipation and heat sink calculation

3.1 Dissipation

The total amount of dissipation in the TDA618JF consists of a sum of two powers.
The first part is the static dissipation, which is the result of the quiescent current and can be calculated with:

Equation 5

$$P_{STAT} = V_{DD} \cdot I_{DD} + 3 \cdot (V_{OCdc} \cdot I_{OCdc})$$

Where:

V_{DD} is the supply voltage.
I_{DD} is the supply current.
V_{OCdc} is the value of the cathode offset.
I_{OCdc} is the value of the dc output current.

The second part is the dynamic dissipation, which is a result of continuously switching of the internal circuitry and thus charging and discharging of on-chip parasitic and load capacitance.
For a sinusoidal signal, it can be calculated with:

Equation 6

$$P_{DYN} = 3 \cdot \left(V_{DD} \cdot C_{TOT} \cdot f_{IN} \cdot V_{OCpp} \cdot \delta \cdot \frac{1}{\sqrt{1 + \frac{f_{IN}}{B_L}}} \right)$$

Where:

V_{DD} is the supply voltage.
C_{TOT} is the sum of the internal- and load capacitance.
f_{IN} Frequency of the input signal.
V_{OCpp} Peak to peak AC component of the output signal.
δ non blanking duty cycle.
B_L Large signal bandwidth of the video amplifier.

This formula however is not representative for a real condition in a TV set. A nominal TV picture consists of a complex variety of signals. If we would use these formulas to calculate a heat sink, the heat sink would be far too big and too expensive. So to calculate a proper heat sink, it is better to see what the video amplifier dissipates in a worst-case condition.

Figure 6 shows the power dissipation as a function of the frequency of a sinusoidal input signal (V_{DD}=200V, V_{OC}dc=100V, V_{OC}=100V_{PP}, δ=0.8, C_L= 20pF)

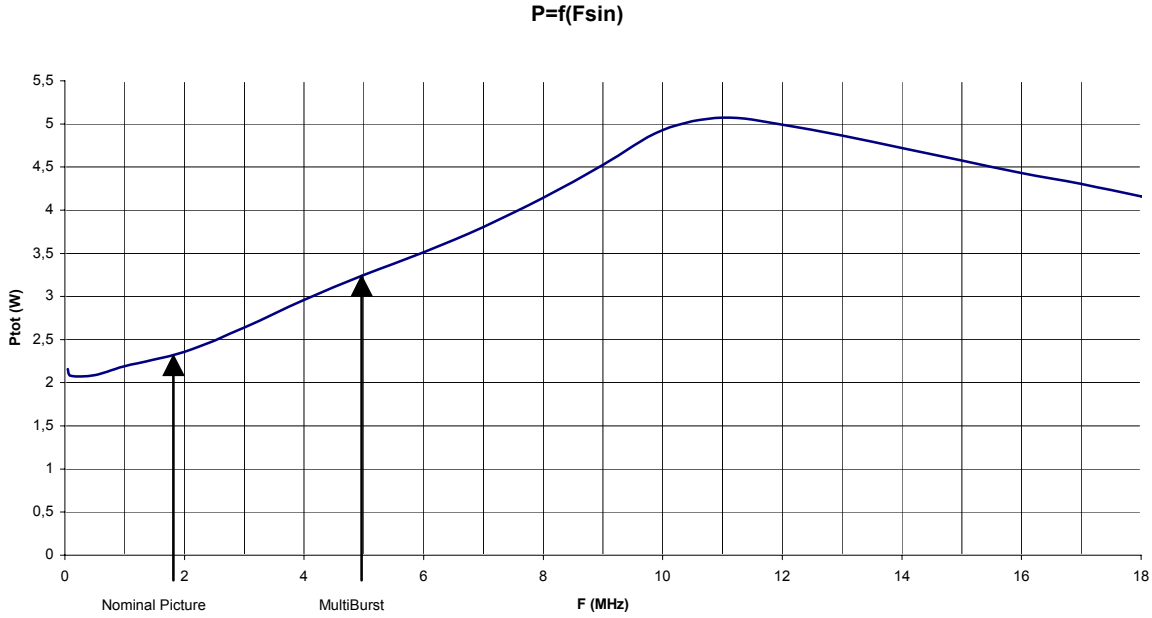

Figure 6: Power as function of the input frequency

As mentioned before, the TDA6118JF is equipped with an internal thermal protection. This circuit gives a decrease of the bandwidth if the temperature of the die is higher than 130°C. This prevents thermal ageing and reduces the necessary heat sink size. Taking this into account the heatsink can be designed for a 'nominal' TV picture (test DVD 1080i, moving content).

3.2 Heatsink calculation

How the heat sink can be calculated is shown underneath.

Equation 7

$$R_{TH,H-A} = \frac{T_{JMAX} - T_A}{P_{TOT}} - \left(R_{TH,J-F} + R_{TH,F-H}\right)$$

Where:

$R_{TH,H-A}$	is the thermal resistance from heat sink to ambient.
$R_{TH,J-F}$	is the thermal resistance from junction to fin.
$R_{TH,F-H}$	is the thermal resistance from fin to heat sink.
T_{JMAX}	is the maximum junction temperature.
T_A	is the ambient temperature in a TV set.
P_{TOT}	is the total of dissipated power.

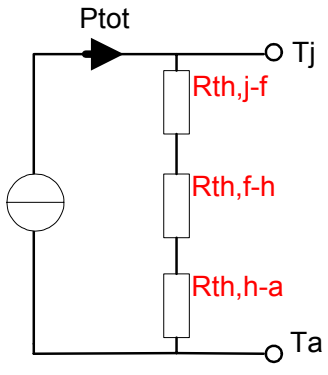

Figure 7: Thermal diagram

The value for $R_{TH,J-F}$ can be found in the datasheet, which is 12.2K/W for the TDA6118JF. The value for $R_{TH,F-H}$ depends on the mounting method and will be under normal conditions about 0.5K/W (if the amplifier is screwed to the heat sink and thermal heat sink compound is used).

T_{JMAX} is the temperature where the internal thermal protection starts to operate, and is approximately 130°C. The maximum ambient temperature in a TV set can be about 65°C.
P_{TOT} can be found in Figure 6 and equals 2.3W, however due to the spread in quiescent supply current we have to add an additional 0.5W so that the power used for calculation will be 2.8W

This results in a heatsink with a thermal resistance of

$$R_{TH,H-A} = \frac{130°C - 65°C}{2.8W} - (12.2°C + 0.5°C) = 10.5K/W$$

When looking at a multiburst during the evaluation of the TDA6118JF, the dissipated power will rise to approximately 3.3W. This results in a die temperature-rise of 78°C, so at an ambient temperature of 25°C the actual die temperature will be 103°C.

To minimise the dissipated power, it is advised to use the supply voltage V_{DD} as low as possible.

4. TDA6118JF APPLICATION & APPLICATION HINTS

In this chapter information is given concerning the application of the TDA6118JF. The circuit diagram of the application of the TDA6118JF is given in Figure 8 below.

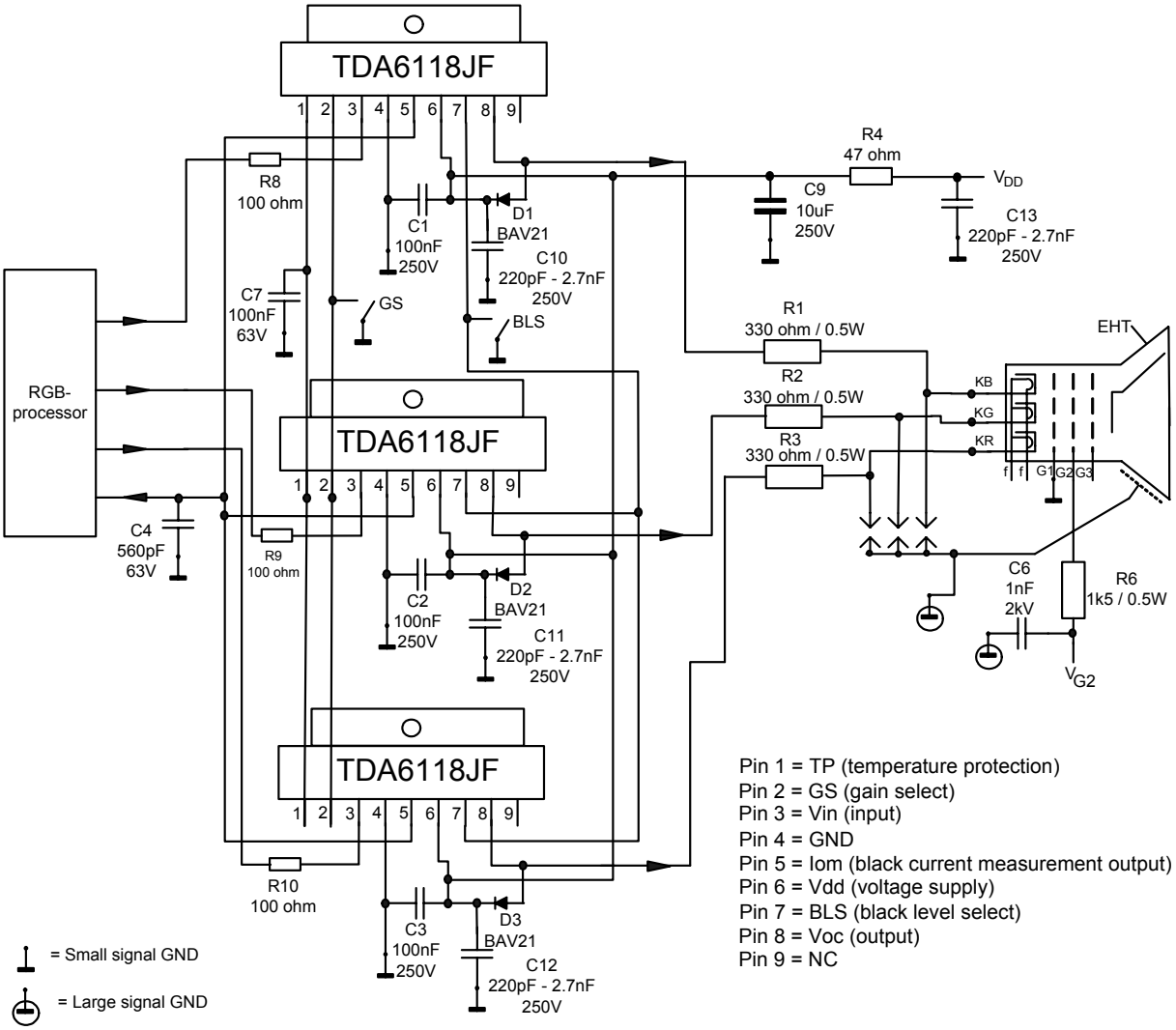

Figure 8: Application diagram of the TDA6118JF

4.1 Design-in sequence of the TDA6118JF

To simplify the design-in of the TD6118JF, the design-in sequence is summarised below:

- Read the cut-off voltage of the CRT in the CRT datasheet.
- Read the nominal value of black level of the RGB-processor.
- Determine the mode for pin 7 BLS (nominal value of the output black level can be 126V or 155V).
- Read the required video drive for the CRT and the available drive from the RGB-processor and calculate the gain.
- Determine the mode for pin 2 GS (gain can be 50 or 80).
- Calculate the power dissipation see section 3.1.
- Calculate the thermal resistance of the required heatsink in section 3.2.

4.2 Interface between RGB-processor and TDA6118JF

The CRT-board is mounted on the neck of the CRT. This means a long (flat) cable must be connected from the RGB-processor output to the input pins of the TDA6118JFs. This results in a capacitive loading of the processor, which can result in a slew rate limitation of the processor. See also the datasheet of the applied RGB-processor. In order to avoid this, a pnp or npn buffer stage can be applied. The best position of this stage is on the main PCB close to the output of the RGB-processor. The simplified diagram is shown in Figure 9.

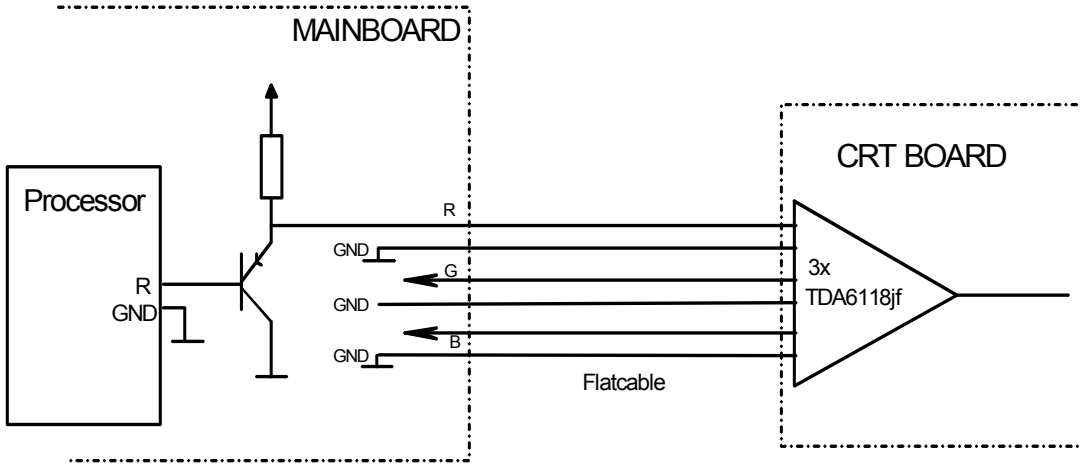

Figure 9: Interface between RGB-processor and TDA6118JF.

The input impedance of the TDA6118JF is rather low ohmic. So it is important to bias the buffer stage sufficiently. Furthermore the input impedance depends on the mode of pin 2 GS.
When pin 2 GS = 0V (gain = 50), the input impedance is typical 1780Ω.
When pin 2 GS = open (gain = 80), the input impedance is typical 1110Ω.

Good stability can be applied with using a flat cable with signal-GND-signal-GND-signal structure. See Figure 9.

4.3 Cross talk and stability

The parasitic links, which could induce cross talk, are shown in Figure 10. The parasitic coupling is caused by parasitic capacitances.

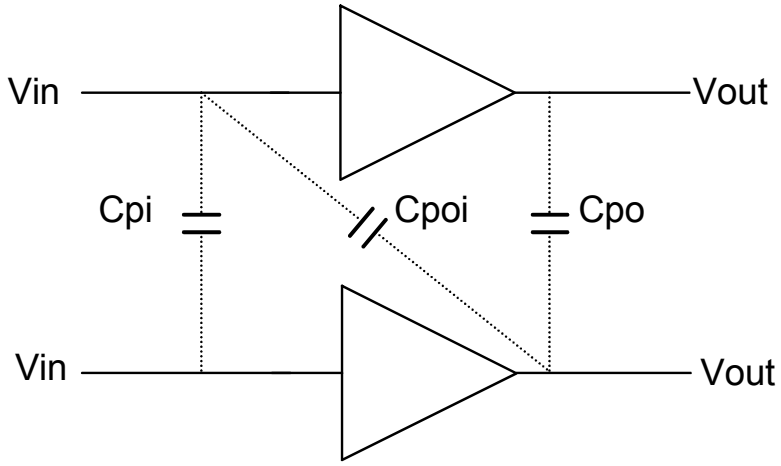

Figure 10: Parasitic capacitors with two video amplifiers.

The cross talk can be caused by:

- Parasitic coupling between the inputs. (Cpi).
- Parasitic coupling between the outputs (Cpo)
- Parasitic coupling between an output and an input of another channel (Cpoi).

The last type of parasitic coupling (Cpoi) is dominant since it involves the coupling of relatively high level output signals with relatively low level input signals. The parasitic coupling between inputs and outputs must be minimised to achieve as low cross talk as possible. This can be done by separating the input and output tracks. Large signal components and wires must be laid out as far as possible from the input signal wires. High frequency signals from the output tracks must not induce a voltage signal at the input of another channel. This can be achieved by a well-designed PCB layout. See Figure 17 for the TDA6118JF reference layout.

Another important cross-talk issue is cross talk related to the current flow in the GND. To avoid cross talk, it is important that output currents can not flow in the ground track of the input part. This goes for the specific channel regarding stability as well as the neighbour channel regarding cross talk. And G1 must be connected directly to pin 4 GND to have good high frequency video signal performance. See Figure 17 for the TDA6118JF reference layout.

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4.4 Switch off behaviour

When a TV set is switched off, the supply voltage V_{DD} becomes low. The output voltage V_{OC} of the TDA6118JF depends on the input voltage V_{IN}. The switch-off behaviour of the TDA6118JF is defined and controllable.

There are two types of switch-off behaviour:

4.4.1 V_{OC} follows V_{DD}, after switch off

The fall time of V_{OC} is determined by the fall time of V_{DD} and can be adapted by the value of the LF decoupling capacitor C9 on V_{DD}. See Figure 11. The minimum value of C9 is limited to 10µF.

4.4.2 V_{OC} is switched to 0V after switch off while Vdd is still high

In this case the CRT will be discharged directly after switch off. See Figure 12.

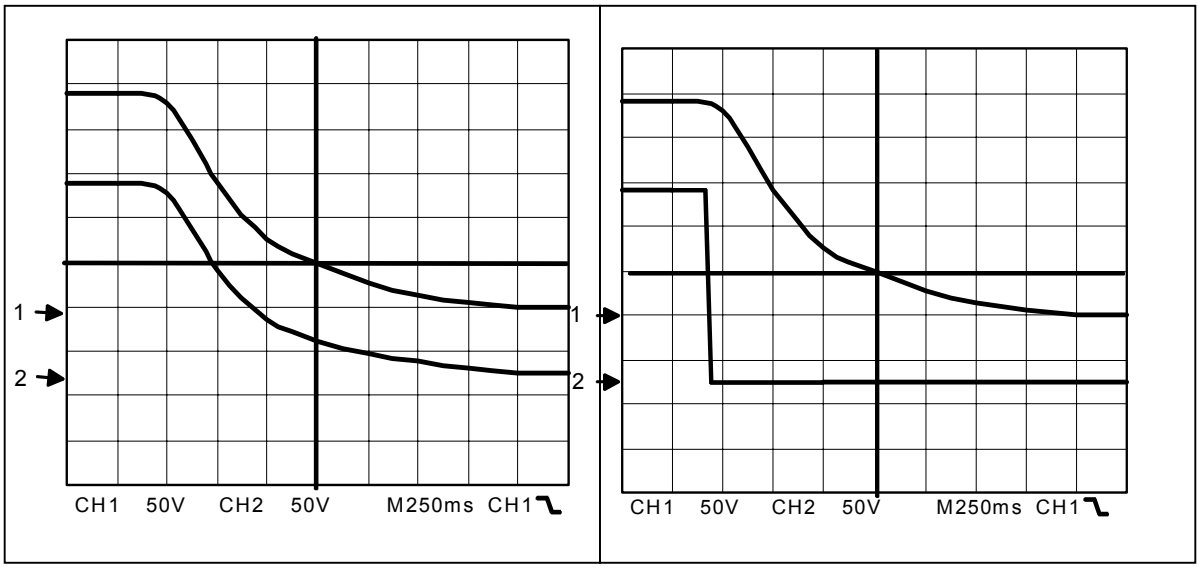

Figure 11: switch off behaviour with V_{OC} follows V_{DD}

Upper trace (CH1): V_{DD} ,50V/div, 250mS/div.
Lower trace (CH2): V_{OC}, 50V/div, 250mS/div.
LF decoupling capacitor on pin 6 V_{DD} C9 = 10µF
C9 = 10µF
The 1 → and 2 → markers show the 0V level.
1→ for the lower trace and 2→ for the upper trace.

Figure 12: V_{OC} is switched immediately to 0V

Upper trace (CH1): V_{DD} ,50V/div, 250ms/div.
Lower trace (CH2): V_{OC}, 50V/div, 250ms/div.
LF decoupling capacitor on pin 6 V_{DD}

5. Flashover protection

A picture tube has generally several high voltage discharges (flashovers) in its lifetime. During the flashovers, a high voltage will be present on the cathodes. The video amplifier must be protected from these flashovers. For optimal flashover protection the grounding wire from aquadag to CRT-board and from CRT-board to main board must be connected like in Figure 13 below.

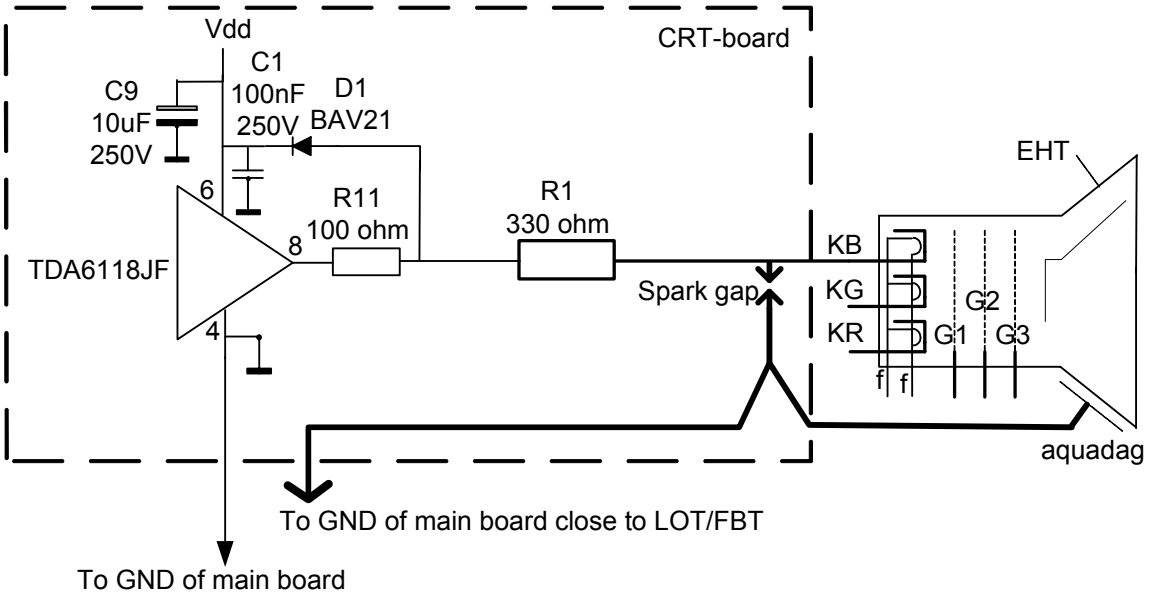

Figure 13: Grounding of aquadag and CRT board.

The video amplifiers need external flash protection to protect against flashovers. The external flash protection consists of an external diode D1 and external resistor R1. The diode clamps the output voltage to the V_{DD}. To limit the diode current an external low ohmic surge resistor R_{FLASH} must be used together with a 2kV spark gap. A more detailed description about the external flash protection is given in the checklist in the next section: 5.1.

5.1 Checklist TDA6118JF for optimal flashover robustness

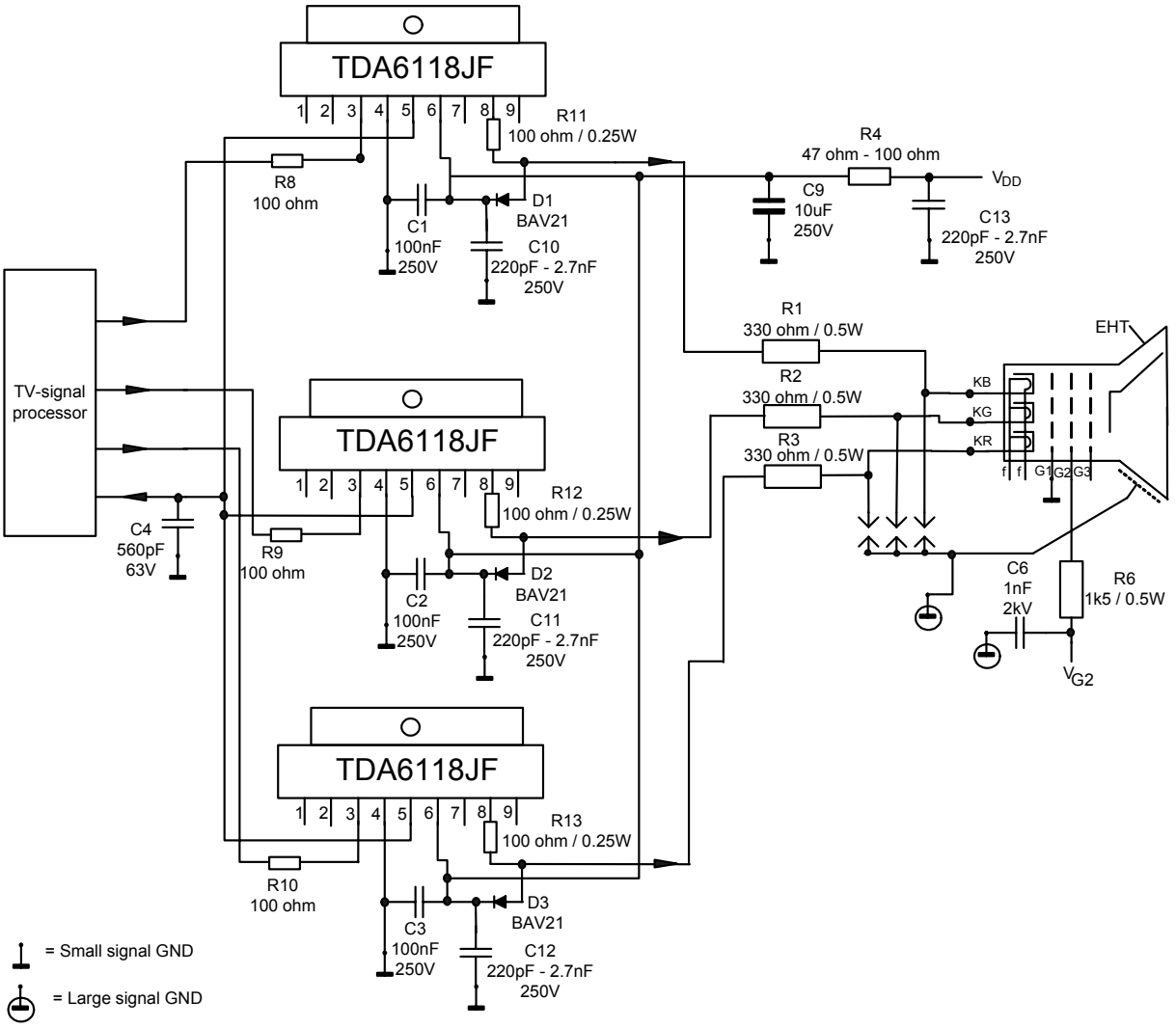

Figure 14: Application diagram of the TDA118JF for optimal flash robustness

Checklist:

	TDA6118JF	Recommended value / type	Explanation
	Grounding of the CRT PCB-layout board		
1.	On the CRT PCB-layout the large signal GND must be isolated from the small signal GND. So pin 4 GND of the TDA6118JF must not be connected directly to the spark gap GND (focus, G2 and cathodes) of the CRT-socket. See Figure 15.		Prevents that large flashover voltage / current peaks can directly flow through the small signal GND.

2.	It is also strongly recommended to place no components (capacitors, resistors and coils) between the small signal GND and the large signal GND. See Figure 15.		Prevents that large flashover voltage / current peaks can directly flow through the small signal GND
3.	Ground loops in the small signal GND must be avoided. So pin 4 GND must have one connection to the connector to the main board. See Figure 15.		Ground loops could reveal in large voltage peaks due to long tracks. V = L*di/dt generated during a flashover
4.	Small signal ground layout must be a star point. See Figure 15.		To avoid GND loops
	External protection components, decoupling circuits		
5.	High frequency decoupling capacitors, C1, C2 and C3	100nF / 250V	C1, C2 and C3 have to reduce fast large voltage peaks between pin 6 V_{DD} and pin 4 GND due to V = L*di/dt. (See points 14 + 15 for optimal PCB layout)
6.	Low frequency decoupling capacitor, C9	10uF / 250V	Low frequency current peaks from a flashover flows via D1, D2 and D3 into C9.
7.	High frequency decoupling capacitors, C10, C11 and C12	220pF - 2.7nF / 250V	C10, C11 and C12 have to reduce fast large voltage peaks between pin 6 V_{DD} and pin 4 GND due to V = L*di/dt.
8.	Series resistor, R4	47Ω - 100Ω / 0.25W	In combination with C10, C11, C12 and C13 for optimal flash robustness
9.	High frequency decoupling capacitor, C13	220pF - 2.7nF / 250V	C13 has to reduce fast large voltage peaks between pin 6 V_{DD} and pin 4 GND due to V = L*di/dt.
	All external capacitors of the TDA6118JF application must be grounded to the **small signal GND**		

The value of C10, C11, C12, C13 and R4 depend on the layout of the CRT-board. During a flashtest can be checked which values give the lowest voltage peaks between pin 6 V_{DD} and pin 4 GND. These voltage peaks can be measured with a digital oscilloscope with probes and grounding as close as possible to pin 6 V_{DD} and pin 4 GND. A special provision can be made on the probe to be close to the pins. It is very important that the grounding wire of the probe is short for not picking up spikes in the GND.

	External protection components, diodes and resistors		
10.	Flash resistors, R1, R2 and R3	330Ω / 0.5W low ohmic surge resistor (high voltage resistor). R1, R2 and R3 must be capable of handling large peak voltages from a flashover	Limits flashover current peaks When the value is larger than 330Ω and R11, R12, R13 have the value of 100Ω, the bandwidth will be smaller than 17Mhz at 100V peak-to-peak output voltage.
11.	Diodes, D1, D2 and D3	BAV21 or equivalent. D1, D2 and D3 must have a fast transient response, low shunt capacitance and capable of handling large peak currents from a flashover	D1, D2 and D3 clamp the output voltage to the V_{DD} voltage supply during a flashover.

12.	Resistors, R11, R12 and R13	100Ω / 0.25W	R11, R12 and R13 have to prevent that the output voltage on pin 8 V_{OC} swings too fast during a flashover.
13.	Resistor, R6	1.5kΩ / 0.5W low ohmic surge resistor. R6 must be capable large peak voltages from a flashover	Limits flashover current peaks on the CRT-board
	Optimal PCB-layout to have optimal robustness		
14.	The cathodes of D1, D2 and D3 must be close to C1, C2 and C3 in the layout. See Figure 15 below.	<5mm	A small discharge loop. The track between diodes and capacitor must be short to avoid high voltages V = L*di/dt generated during a flashover.
15.	C1, C2 and C3 must be as close as possible to pin 4 V_{DD} and pin 6 GND See Figure 15 below.	<5mm	Prevent that large flashover voltage / current peaks can directly flow through the small signal GND.
16.	Distance of G2, G1, R, G, B copper tracks to adjacent tracks	> 3 mm	Prevent arcing during flash over.
17.	G2 CRT pins must have 2 slots cut on the PCB to increase the distance from the adjacent R and B pins.		Prevent arcing during flash over.
18.	No copper track in between CRT pins.		Prevent arcing during flash over.
19.	No sharp edges on the copper track.		Prevent arcing during flash over.
20.	Large signal GND and (if used) EHT info track distance must be 2mm from all other tracks.	> 2mm	Prevent arcing during flash over.
21.	CRT wire between aquadag layer and CRT-board must be as short as possible.		A small discharge loop during flashover.
22.	CRT wire between aquadag layer and CRT-board must not be too thin.		Low impedance discharge loop during flashover.

Figure 15 shows the optimal CRT PCB-layout for protection against flashover.

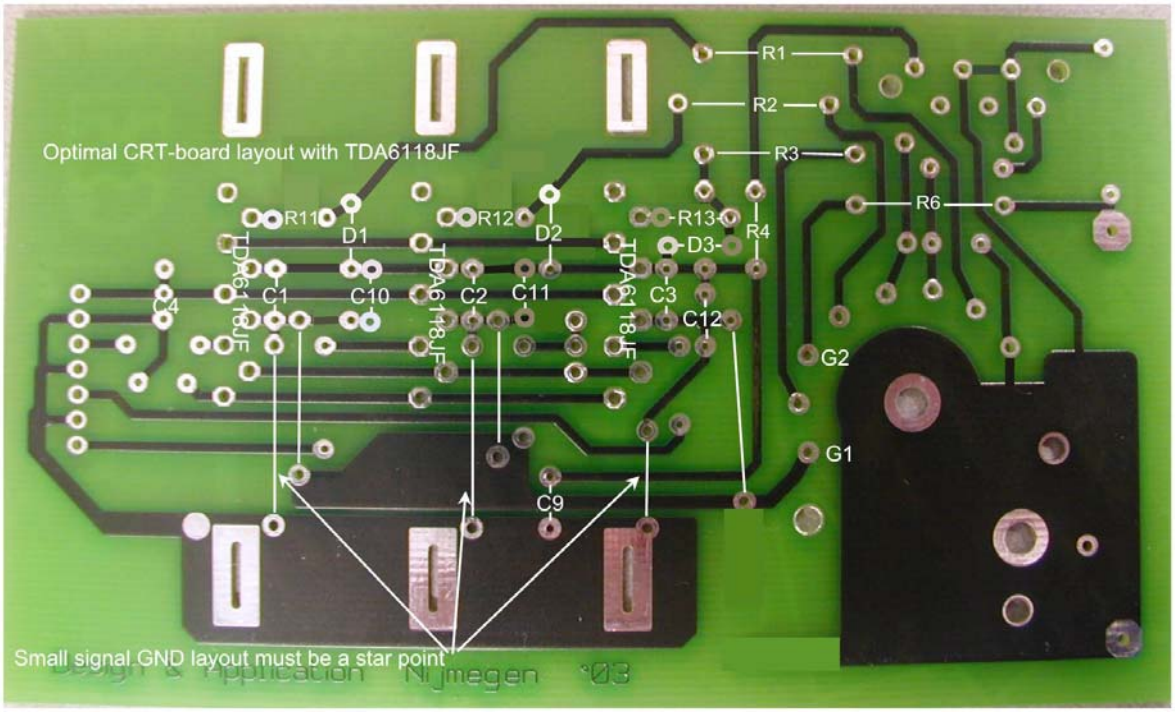

Figure 15: Optimal CRT PCB-layout with TDA6118JF

6. The TDA6118JF reference / demo board.

The TDA6118JF reference / demo board shown in Figure 17, Figure 18 and Figure 19 is meant for evaluation and demonstration purposes. The CRT base socket is JEDEC B10-277. This reference board of the TDA6118JF is constructed with single-sided copper.

To get the optimal performance, special attention has to be paid on the following points of the PCB layout. See also section 4.3.

- Keep high frequency current loops as short as possible.
- Separate large and small signal current paths.
- Minimise parasitic capacitance; keep hf-signal tracks as narrow as possible.
- Use star point grounding, make ground and supply tracks as wide as possible.

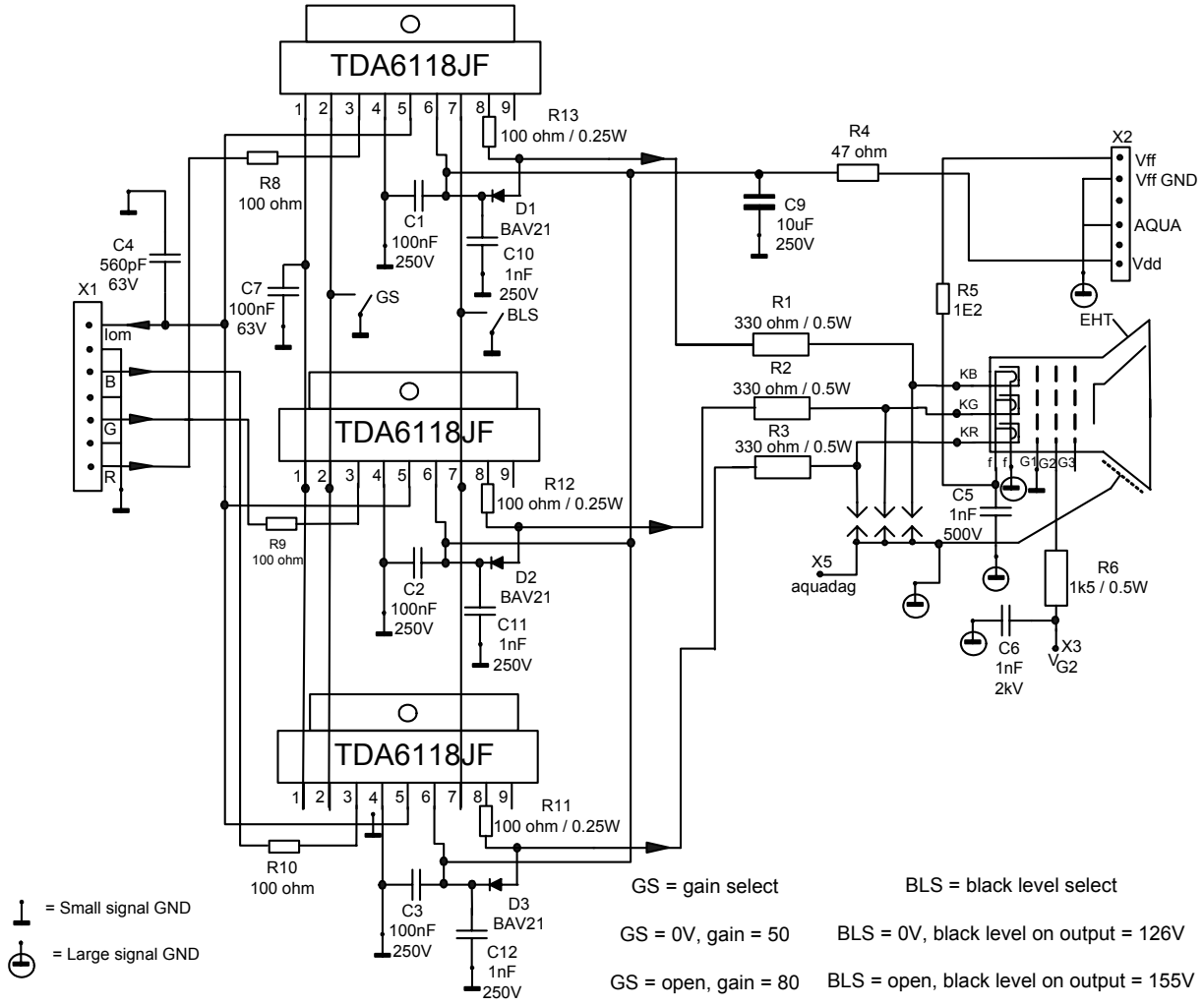

Figure 16: Application diagram of the TDA6118JF reference / demo board.

PART LIST

Position	VALUE	RATING	TYPE
IC			TDA6118JF
C1, C2, C3	100nF	250V	MKT
C4	10µF	250V	elcap
C5	2.7nF	500V	ceramic
C6	1nF	2000V	ceramic
C7	100nF	63V	MKT
C10, C11, C12	1nF	500V	ceramic
R1, R2, R3	330Ω	0.5W	low ohmic surge / high voltage
R4	47Ω		NFR25
R5	1.2Ω	0.25W	SFR16
R6	1k5	0.5W	low ohmic surge / high voltage
R8, R9, R10	100Ω	0.25W	SFR16
R11, R12, R13	100Ω	0.25W	SFR16
D1, D2, D3			BAV21
X1			6-pole connector
X2			7-pole connector
Picture tube socket with integrated spark gaps			JEDEC B10-277

TDA6118JF reference / demo board (layout side)

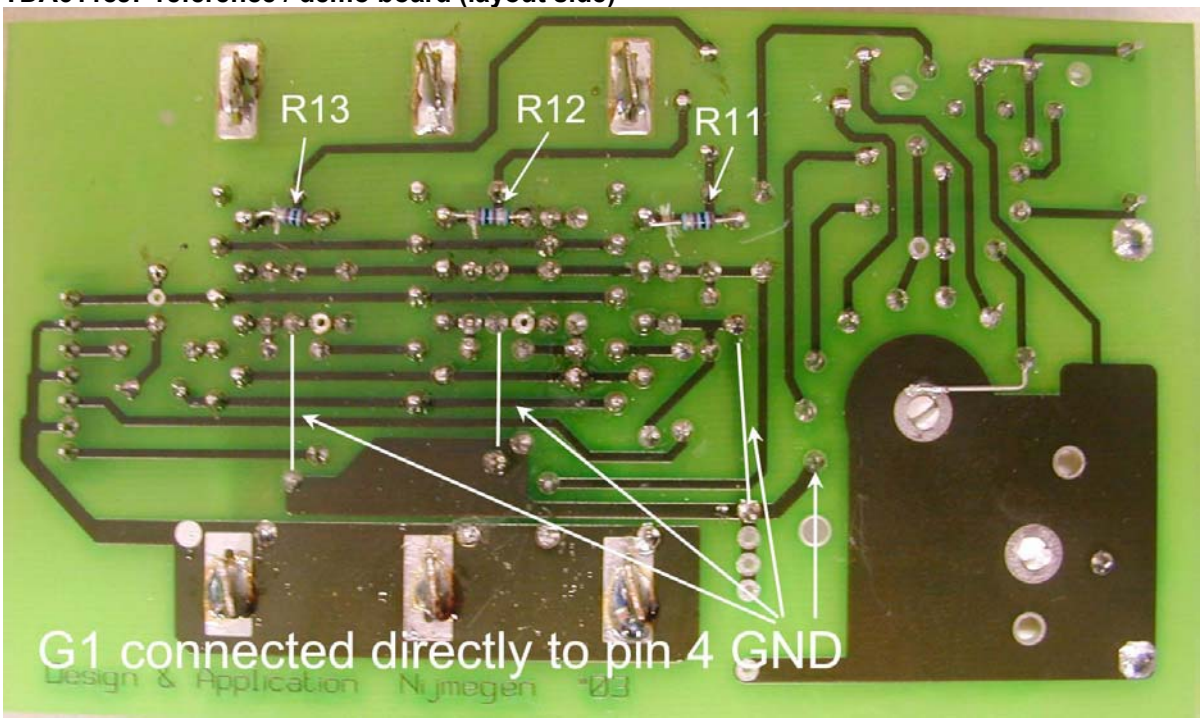

Figure 17: TDA6118JF reference / demo board layout

TDA6118JF reference / demo board (component side)

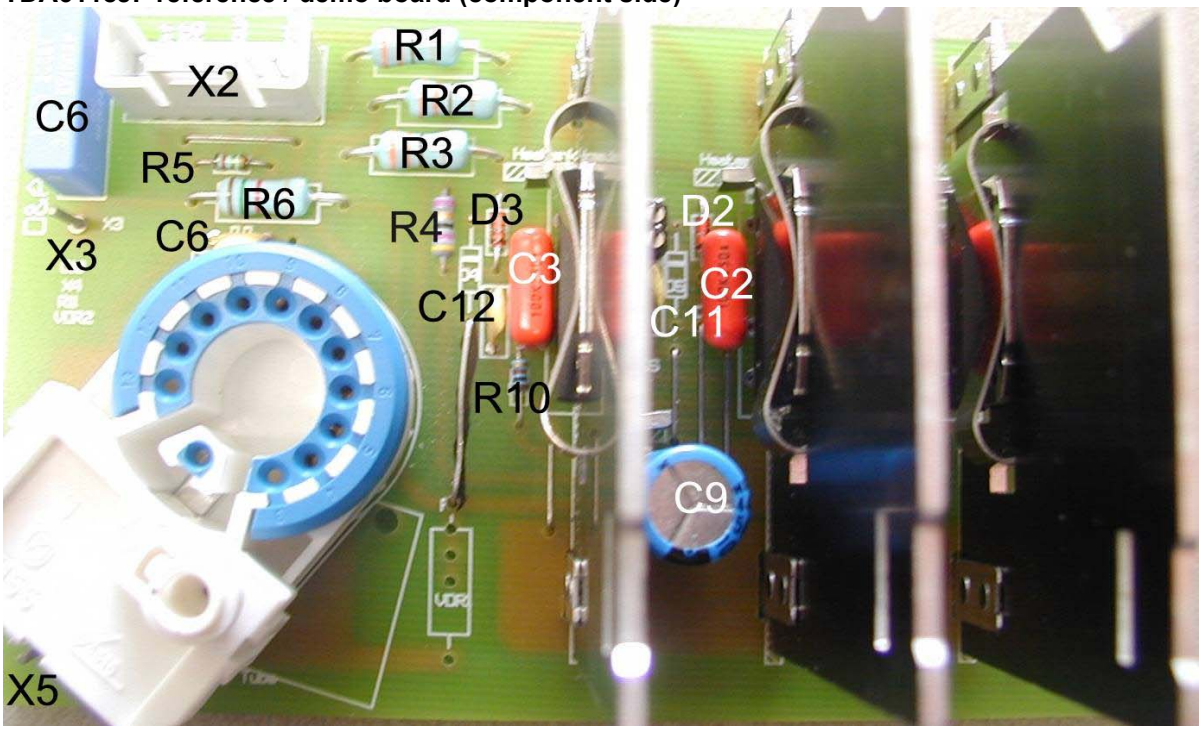

Figure 18: Components TDA6118JF reference / demo board

TDA6118JF reference / demo board (component side)

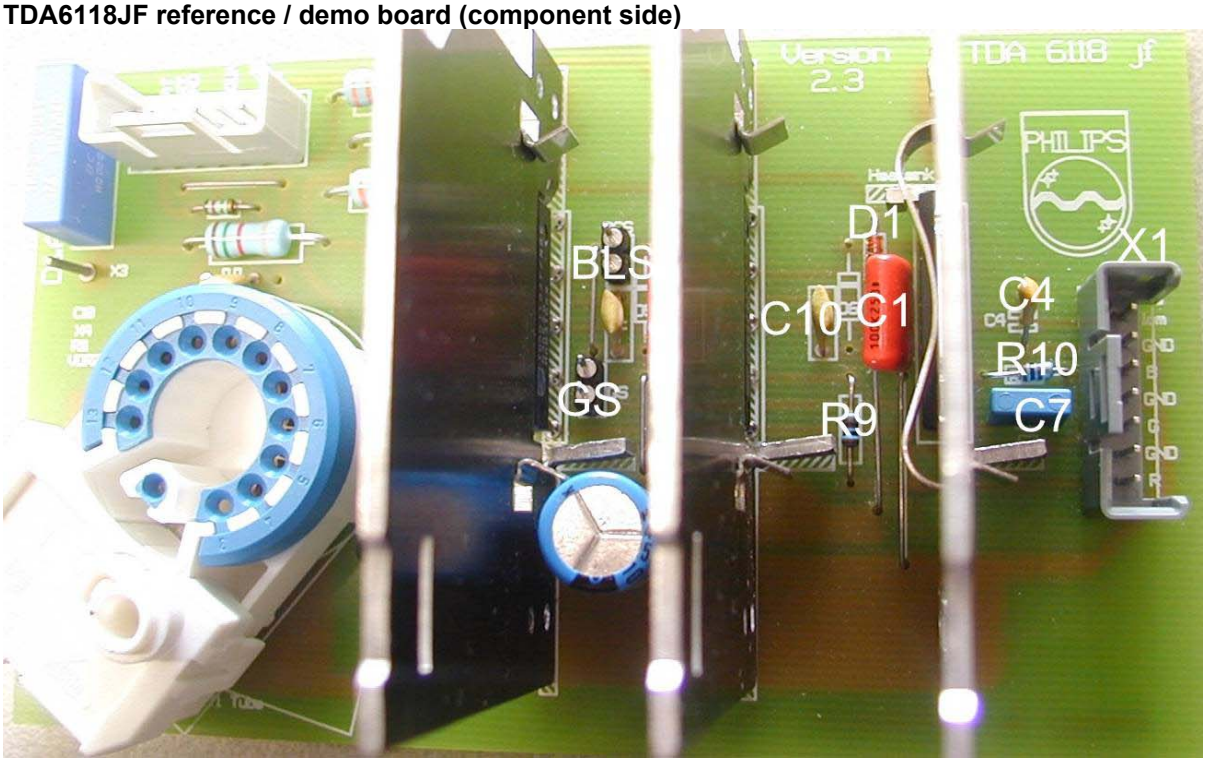

Figure 19: Components TDA6118JF reference / demo board (2)

7. TDA6118JF interface socket for a TDA6120Q application

When a set is equipped with the TDA6120Q video amplifier, a **TDA6118JF interface socket** can be used to for a quick evaluation of the TDA6118JF. The TDA6118JF has an internal fixed reference voltage of 2.5V.

The TDA6120Q however has an external reference voltage, which can vary between 1.5V and 5V.

If the reference voltage of the TDA6120Q is not equal to 2.5V this will result in an incorrect black level output voltage of the TDA6118JF. It is possible to correct this difference by means of adapting the dc level of the input of the TDA6118JF.

The circuit diagram and the layout are given below in Figure 20 and Figure 21.

Guidelines for a quick implementation of the TDA6118JF interface socket:

1. Remove the TDA6120Q video amplifiers from the CRT-board.
2. Insert the TDA6118JF interface socket in the TDA6120Q position pins. See Figure 20.

Connect pins 1 TP of the 3 TDA6118JF amplifiers together by means of a wire to obtain thermal protection synchronisation. See

3. Figure 22.
4. Connect a heatsink on the TDA6118JF amplifiers.

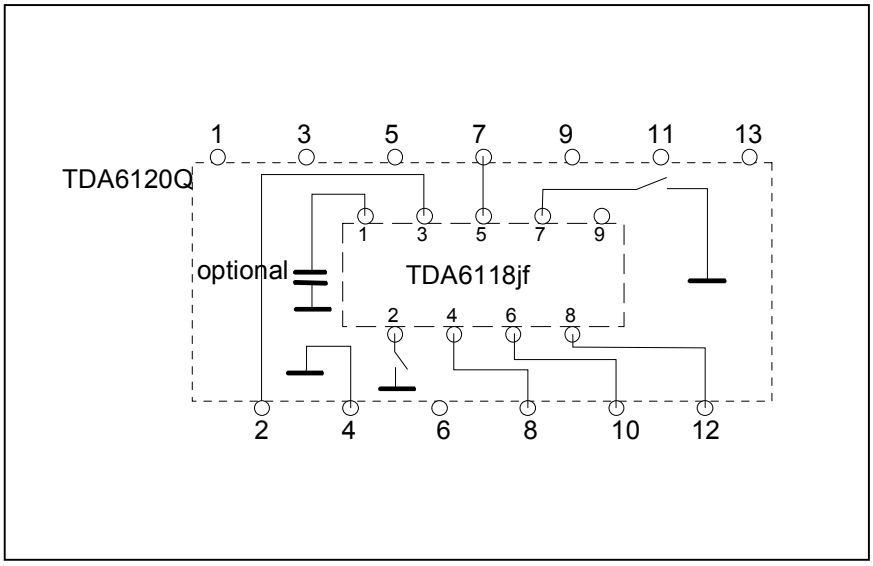

Figure 20: Electrical interface diagram TDA6120Q to TDA6118JF

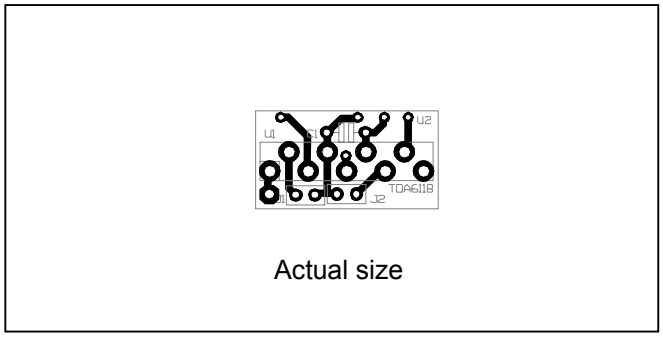

Figure 21: Layout of the interface board

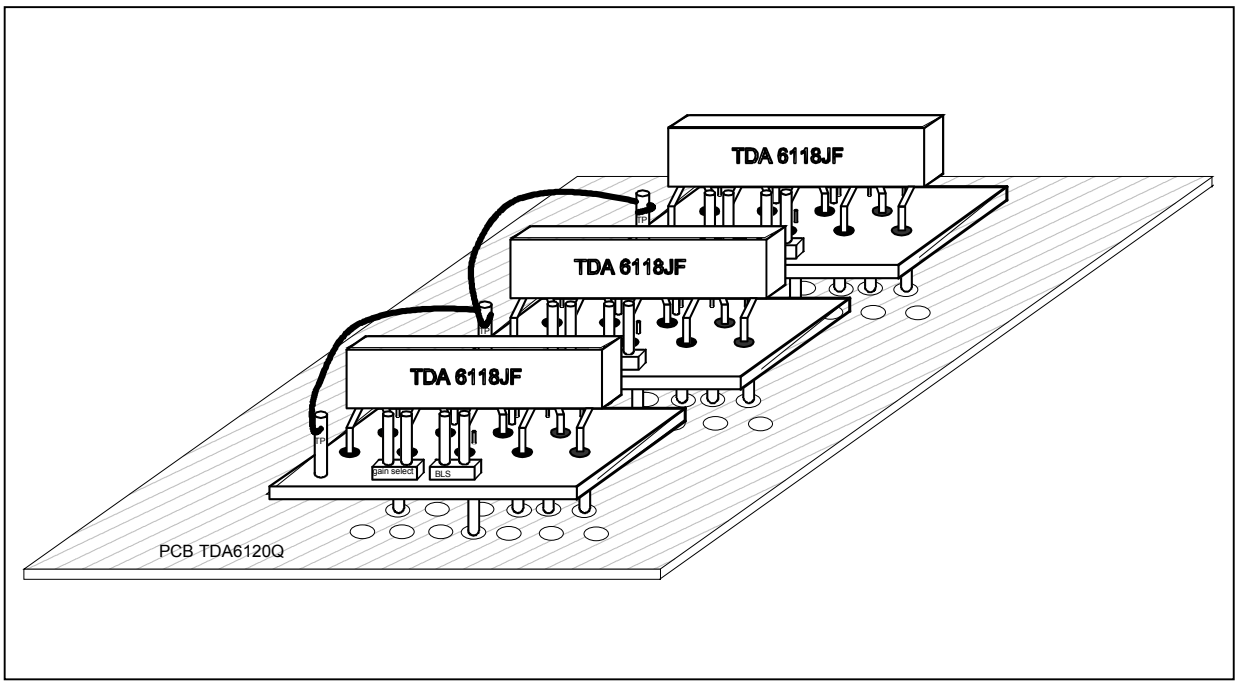

Figure 22: 3D-View of the inserted TDA6118JF interface sockets

8. APPENDIX

1) Derivation of influence of the value of RA on the voltage gain
2) Derivation of influence of the value of RA on the cut-off voltage

8.1 Appendix A

Derivation of influence of R_A on voltage gain

The voltage gain of an amplifier is given by

$$Av = \frac{\delta Vout}{\delta Vin}$$

Because of the high impedance of the inputs, there will not flow any current into the opamp, therefore we can state that

$$\varepsilon = 0$$

So we can conclude that

$$V^{-} = Vref$$

According to Kirchhoff's current law we can write

$$\frac{Vout - Vref}{Rf} + \frac{Vin - Vref}{Ri} = \frac{Vref}{Ra}$$

Writing out this equation results in

$$\frac{Vout}{Rf} - \frac{Vref}{Rf} + \frac{Vin}{Ri} - \frac{Vref}{Ri} = \frac{Vref}{Ra}$$

Which can be rewritten into

$$\frac{Vout}{Rf} + \frac{Vin}{Ri} = \frac{Vref}{Ra} + \frac{Vref}{Rf} + \frac{Vref}{Ri}$$

Isolating V_{REF} results in

$$\frac{Vout}{Rf} + \frac{Vin}{Ri} = \left(\frac{1}{Ra} + \frac{1}{Rf} + \frac{1}{Ri}\right) \cdot Vref$$

Now its easy to find an equation for V_{OUT}

$$\frac{Vout}{Rf} = \left(\frac{1}{Ra} + \frac{1}{Rf} + \frac{1}{Ri}\right) \cdot Vref - \frac{Vin}{Ri}$$

$$Vout = \left\{\left(\frac{1}{Ra} + \frac{1}{Rf} + \frac{1}{Ri}\right) \cdot Vref - \frac{Vin}{Ri}\right\} \cdot Rf$$

As mentioned in before, we can derive the voltage gain

$$\frac{\delta Vout}{\delta Vin} = \frac{\delta\left\{\left(\frac{1}{Ra}+\frac{1}{Rf}+\frac{1}{Ri}\right)\cdot Vref - \frac{Vin}{Ri}\right\}\cdot Rf}{\delta Vin}$$

The differentiated value of a constant value is zero, so

$$\frac{\delta Vout}{\delta Vin} = \frac{\delta\left\{-\frac{Vin}{Ri}\right\}\cdot Rf}{\delta Vin}$$

Rewriting makes it easier

$$\frac{\delta Vout}{\delta Vin} = \frac{\delta Vin\cdot\left\{-\frac{Rf}{Ri}\right\}}{\delta Vin}$$

Finally this results in

$$Av = \frac{\delta Vout}{\delta Vin} = -\frac{Rf}{Ri}$$

Now we can conclude that the gain only depends on R_F and R_I, thus independent of R_A

8.2 Appendix B

Derivation of influence of R_A on $V_{OUTblack}$

The voltage gain of an amplifier is given by

$$Av = \frac{\delta Vout}{\delta Vin}$$

Because of the high impedance of the inputs, there wont flow any current into the opamp, therefore we can state that

$$\varepsilon = 0$$

So we can conclude that

$$V^{-} = Vref$$

According to Kirchhoff's current law we can write

$$\frac{Vout - Vref}{Rf} + \frac{Vin - Vref}{Ri} = \frac{Vref}{Ra}$$

Writing out this equation results in

$$\frac{Vout}{Rf} - \frac{Vref}{Rf} + \frac{Vin}{Ri} - \frac{Vref}{Ri} = \frac{Vref}{Ra}$$

Which can be rewritten into

$$\frac{Vout}{Rf} = \frac{Vref}{Ra} + \frac{Vref}{Rf} - \frac{Vin}{Ri} + \frac{Vref}{Ri}$$

If V_{IN} equals V_{REF} (thus at picture tube cut-off) we can write

$$\frac{Vout}{Rf} = \frac{Vref}{Ra} + \frac{Vref}{Rf} - \frac{Vref}{Ri} + \frac{Vref}{Ri}$$

Isolating V_{OUT} results in

$$Vout = \frac{Vref \cdot Rf}{Ra} + \frac{Vref \cdot Rf}{Rf} - \frac{Vref \cdot Rf}{Ri} + \frac{Vref \cdot Rf}{Ri}$$

Next, isolating V_{REF} results in

$$Vout = Vref\left(\frac{Rf}{Ra} + 1\right)$$

Since R_F is fixed, its clear that $V_{OUTblack}$ depends on the value of R_A

9. REFERENCES

1. Datasheet TDA6118JF.
2. Application of the TDA6120Q wide band video output amplifier –AN96073- by: E.H. Schutte.

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